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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,139	09/09/2003	Shinji Ohuchi	KKH.039D2	1910

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EXAMINER

NGUYEN, DILINH P

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Specification

The abstract of the disclosure is objected to because it includes reference characters.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 34-38 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (U.S. Pat. 5,239,198)..

Lin et al. (figs. 6-7) disclose a semiconductor device comprising:

a BGA (ball grid array) 52 type semiconductor device including a base plate 12 and a plurality of bumps 32 formed on a backside surface of the base plate; and

a CSP (chip size package) type semiconductor device mounted on an area of the backside surface of the base plate of the BGA type semiconductor device which does not have any bumps formed thereon,

the CSP type semiconductor device having a semiconductor element 50 which has main and back surfaces, and side surfaces between the main and back surfaces, and a plurality of terminals (a plurality of pads formed on the element 51 or on the chip 50) which are formed on the main surface,

wherein the back surface and the entirety of the side surfaces of the semiconductor element are exposed (figs.6- 7, column 6, lines 55 et seq.).

- Regarding claim 35, Lin et al. disclose that the plurality of terminals 51 of the CSP type semiconductor device are electrically connected to the plurality of bumps 32 (fig. 7) via wiring patterns 16 formed on the backside surface of the base plate (fig. 6, column 6, lines 61-65).
- Regarding claim 36, Lin et al. disclose that the plurality of terminals of the CSP type semiconductor device are coupled to the wiring patterns via solder joint 51 (fig. 7).
- Regarding claim 37, Lin et al. disclose that the CSP type semiconductor device is mounted on the BGA type semiconductor device so that a front surface of the CSP type semiconductor device faces the backside surface of the base plate 12 (fig. 7).
- Regarding claim 38, Lin et al. disclose that the backside surface of the base plate is mounted to a printed circuit board 38 (column 5, line 65) via the plurality of bumps 32, and the CSP type semiconductor device as mounted on the backside surface of the base plate has a thickness less than a thickness of the plurality of bumps 32 (fig. 7).
- Regarding claim 46, Lin et al. disclose that the main surface of the semiconductor element faces the backside surface of the base plate (fig. 7).

Claim Rejections - 35 USC § 103.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 45 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. 5239198) (previously applied) in view of Schrock (U.S. Pat. 5,861,678) (previously applied).

Lin et al. fail to disclose a resin that covers the main surface of the semiconductor element and side surface of the terminals.

However, Schrock discloses a CSP type semiconductor device 10 has a resin 40 that covers the main surface of the semiconductor element and side surfaces of the terminals 44 (figs. 4a-4b, column 4, lines 33-58). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Lin et al. by having the resin layer that covers the main surface of the CSP, as taught by Schrock, for firmly secure the die to the substrate (column 5, lines 62-65).

- Regarding claim 47, Lin et al. disclose that the main surface of the semiconductor element faces the backside surface of the base plate (fig. 7).

Allowable Subject Matter

Claim 53 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 8/9/05 have been fully considered but they are not persuasive.

- The applicant argues that element 50 of the Lin et al. reference is a passive electronic component, such as a resistor, a diode, a decoupling capacitor, or the like. Lin et al. reference does not describe passive electronic component 50 as a semiconductor device.

Applicant's argument has been fully considered but it is not persuasive because the passive electronic component element 50 (resistor, diode, decoupling capacitor) is a semiconductor device. Note Nishi et al. (U.S. Pat. 5949140) Col. 9, lines 24-27; and Lee et al. (U.S. Pat. 6081037) Col. 1, lines 54-57 are cited to support for the well known position.

- The applicant argues that passive electronic component 50 of the Lin et al. reference is not a CSP.

Applicant's argument has been fully considered but it is not persuasive because the passive electronic component 50 of the Lin et al. reference is a semiconductor chip comprises a plurality of solder balls 51 (fig. 7, column 6, lines 64). Therefore, Lin et al. clearly disclose that the component 50 is a Chip Scale Package (CSP) type.

- In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., high density packaging, a high performance device utilizing and small high density package, as in claim 34) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
- In response to applicant's argument that there is no motivation to combine the references, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).
- The applicant argues that Schrock reference is not specifically described as a BGA and a plurality of bumps formed on a backside surface of the base plate, as would be necessary to meet the features of claim 34.

The applicant arguments have been fully considered but they are not persuasive because this argument has no immediate apparent relevance to the issues presented by the rejection before us since an applicant cannot show nonobviousness by attacking references individually wherein the rejection is based upon a combination of references. In re Young, 403 F. 2d 754,757,159 USPQ 725, 728 (CCPA 1968).

It should be noted that the rejection of claims 45 and 47 are not based on anticipation, but rather, is based on obviousness.

Examiner relies on the combined teachings at Lin et al. and Schrock. Schrock is relied on for showing a resin that covers the main surface of the semiconductor element and side surface of the terminals. The Examiner thus regards the applicant assertions as constituting evidence that The Applicant has failed to consider as a whole the prior art teachings disclosed by the combining of the references.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

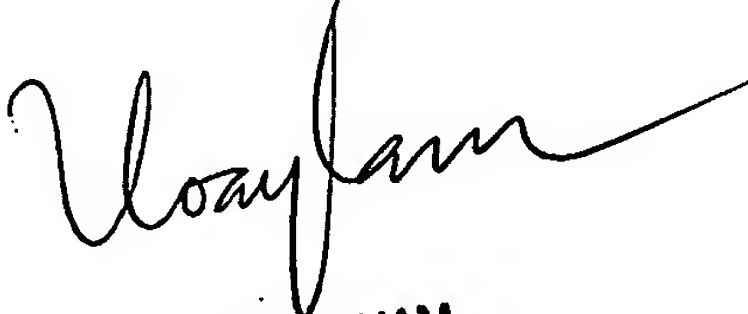
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN



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PRIMARY EXAMINER